REMARKS

Claims 1-15 are pending in this Application, of which Claims 1, 9, 13 and 14 are the independent claims. All claims stand rejected.

Claims 9 and 13 have been objected to for reciting "the delay circuit" without antecedent basis. Accordingly, claims 9 and 13 are being amended to recite "a delay circuit providing the delay" and "means including a delay circuit," respectively. As a result, the objection to claims 9 and 13 is believed to be overcome, and acceptance is respectfully requested.

Claims 16-19 are being added. Support for these claims is found at least in Fig. 4 and on page 9, lines 5-16 of the Specification as originally filed. Acceptance is respectfully requested.

Rejection of Claims 1-15 under 35 U.S.C. § 103 and § 102

Claims 1-13 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin et al. (US Pub No. 2007/0007941) in view of Birru (US Patent No. 6,215,343). Claims 14 and 15 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Birru. Applicant respectfully disagrees with these rejection for the reasons set forth below, and reconsideration is requested.

Applicant agrees with the assertion at page 3 of the Office Action that Lin does not teach an "initialization circuit" as recited in claims 1 and 13. Yet, contrary to the Office Action, Birru also fails to teach an initialization circuit that "after reset of the delay locked loop assures that the phase detector initially changes the delay in a direction away from a first end of the delay range after receipt of one of the reference clock and feedback clock and enables a change in the delay in an opposite direction toward the first end only after receipt of one of the reference clock and feedback clock followed by receipt of the other of the reference clock and feedback clock."

Referring to Birru at Figs. 3 and 4, Birru discloses circuits to address a "false lock" error that results in a delay-locked loop (DLL) locking "at an undesired integral multiple of 360 degrees" (Birru, col. 1, lines 25-40). With reference to Fig. 1, this error can occur when the delay elements DL1-DLN in the DLL have different delay values upon startup of the DLL. As a result, the phase comparator PHCMP may achieve a lock between the clock phi0 and delayed

clock phiN at an incorrect phase interval. Birru describes how this error occurs in detail at col. 4, lines 21-53, with reference to Fig. 6.

Birru's circuits at Figs. 3 and 4 prevent "false lock" error by disabling phase control signals upon startup of the DLL until specific conditions are detected. As shown in Figs. 3 and 8, an initialization flip flop IFF and Flip-flops FF1-FF3 delay the onset of signals DD and ID, respectively. For example, signal ID is disabled until each of the delay elements DL (Fig. 1) are clocked in sequence by flip-flops FF1-FF3. As a result, the DLL delay can be decreased until the delayed clock phi4 is the desired integral multiple of 360 degrees of the reference clock phi0 (col. 5, line 64 – col. 6, line 31).

After enabling delay adjustment in one direction, Birru does not enable "a change in the delay in an opposite direction ...only after receipt of one of the reference clock and feedback clock followed by receipt of the other of the reference clock and feedback clock," as recited in Claim 1. As shown in Fig. 7, Birru enables control signal ID after 1) each of the flip-flops FF1-FF3 (Fig. 3) is clocked in sequence by a respective one of the delay elements (Fig. 1), and 2) the delayed clock phi4 goes "high" (col. 5, lines 45-63). Even if phi4 were considered a "feedback clock," Birru fails to provide for requiring a reference clock before enabling a change in delay. After control signal DD is enabled, only the delayed clock signal is received before the control signal ID is enabled; the reference clock phi0 is not enabled during this time. In contrast, the above claim language requires that both the reference clock and the feedback clock are received before enabling a change in delay in the opposite direction. Birru provides no such requirement, and instead relies on an entirely different control logic as described above. It should be noted that the timing diagrams of Figs. 7 and 8 correspond to the circuit shown in Fig. 3, and the circuit in Fig. 4 provides similar functionality as the circuit of Fig. 3 using fewer flip-flops (col. 6, lines 33-40). Thus, Birru does not disclose an initialization circuit as recited in Claims 1 and 14; nor does it disclose the "assuring" and "enabling" operations as recited in Claims 9 and 13.

The Office Action further asserts that Birru's circuit in Figs. 3-4 is similar to Applicant's initialization circuit 410 in Fig. 4 of the Specification. However, these circuits are distinct. For example, Applicant's flip-flop 404 is clocked by the reference clock (CLK_REF), and its output signal is received by flip-flops 403, 402, both of which are clocked by the feedback clock (CLK_FB). In contrast, Birru's flip-flop IFF is clocked by reference clock phi0, but its output

signal Q0 is received by flip-flops BFF1, FF1, which are clocked by either the reference clock phi0 or another delayed clock phi2, and are not clocked by the feedback clock. Thus, one skilled in the art would, by way of straightforward and precursory review of the circuitries implementing the circuits in question, clearly understand that Birru's circuits differ functionally from the circuits 400 shown in Fig. 4, such that the initialization circuit as recited in claims 1 and 14, as well as the methods recited in claims 9 and 13, are not disclosed in Birru.

Claims 2-8, 10-12 and 15 depend from one of claims 1, 9 and 14 and thus are allowable at least for the reasons indicated above. As a result, the § 103 and § 102 rejections of Claims 1-15 are believed to be traversed, and reconsideration is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By _____
Benjamin J. Sparrow
Registration No. 62,259
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Date: 6/10/08